Yield Learning and Volume Manufacturing of High Performance Logic Technologies On 200mm and 300mm Wafers

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Abstract

This paper describes the rapid yield learning and high volume ramp of Intel's 130nm logic technology on both 200mm and 300mm wafers. This process technology delivers industry leading performance, yield, reliability and density that is matched on both 200mm and 300mm wafers. This technology supports SRAM cell sizes down to 2µm^2 and has produced >10M high speed microprocessors at the time of this publication.

Introduction

In 1965 Gordon Moore observed that transistor density doubled every 18 months (1). "Moore's Law" is driven by the recognition that competition is established by delivering process technologies on "the leading edge" of performance and density in high volumes. Figs. 1 and 2 show that for more than the past six technology generations Intel has ramped high performance logic technologies at continuously increasing rates and ever improving yield levels even though the technology introduction cycle time has been shrinking.

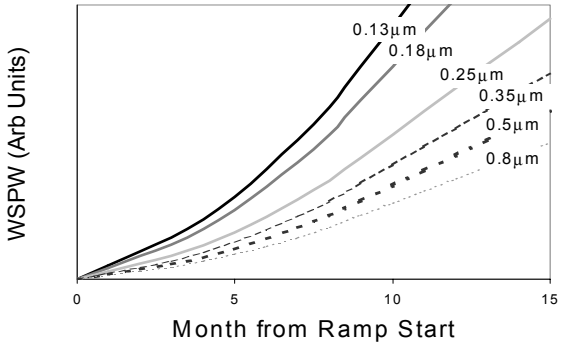


Figure 1. Intel Initial High Volume Manufacturing Ramp Rates

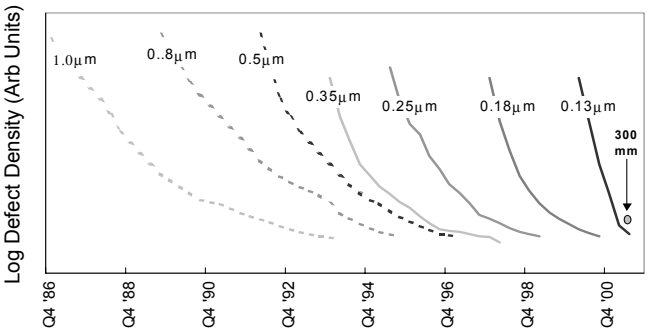


Fig 2. Intel Logic Technology Defect Density Trends

High Performance 130 nm Logic Technology

Most recently, Intel has led the industry in early 2001 with the high volume manufacturing ramp of a 130nm technology featuring high performance 70nm dual Vt transistors, copper and low k dielectric interconnect and 2µm^2 SRAM cell size (2). Table 1 summarizes design rules for this technology. Figs. 3 and 4 show Pentium ™ III die and relative performance for 130nm and 180nm process technologies.

TABLE 1
130nm TECHNOLOGY DESIGN RULE SUMMARY

LAYER	PITCH (NM)	THICK (NM)	AR
Isolation	345	450	-
Polysilicon	319	160	-
Metal 1	293	280	1.7
Metal 2, 3	425	360	1.7
Metal 4	718	570	1.6
Metal 5	1064	900	1.7
Metal 6	1143	1200	2.1

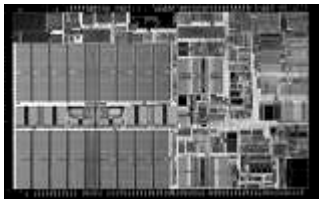


Figure 3. Pentium™ III Die on 130nm Technology

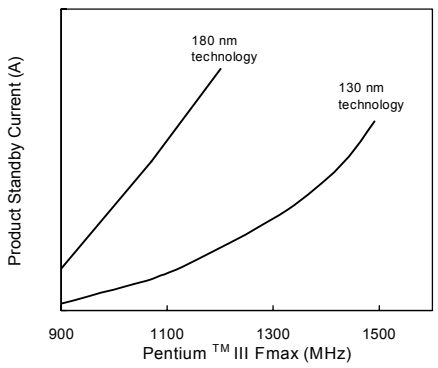


Figure 4. Comparison of Pentium™ III Performance on 180nm and 130nm Process Technologies

Process Design for Manufacturing and Performance

A. Design for Process Capability

In order to enable rapid ramp of the technology in numerous high volume manufacturing fabs, the process technology must be highly capable and stable. Fig. 5 shows the process capability distribution for in-line "key process monitors" that predict the performance, yield and/or reliability for the 0.25, 0.18 and 0.13µm logic technology generations at Intel (at two year offsets). With each successive generation process capability, stability and excursion resistance at the start of high volume ramp have improved. Fig. 6 shows how Intel develops proprietary chemistries, such as Cu plating chemistries, to enhance yield and manufacturability. Design for manufacturing (DFM) techniques are utilized, which make extensive use of error analysis in setting process targets (3). Finally, extensive excursion protection, statistical process control (SPC) capability has been designed into the shop floor control system, which enables early detection of proc-

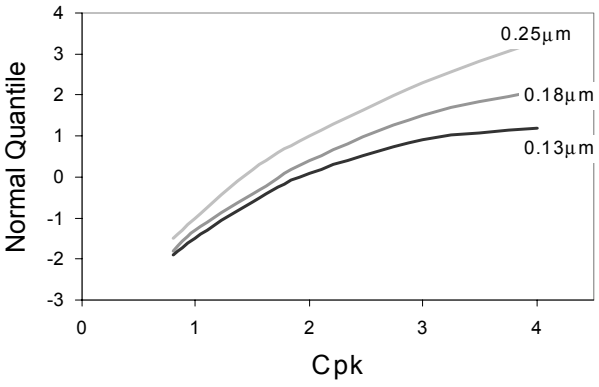


Figure 5. Process Capability Distributions for Intel Technologies at Start of High Volume Manufacturing Ramp

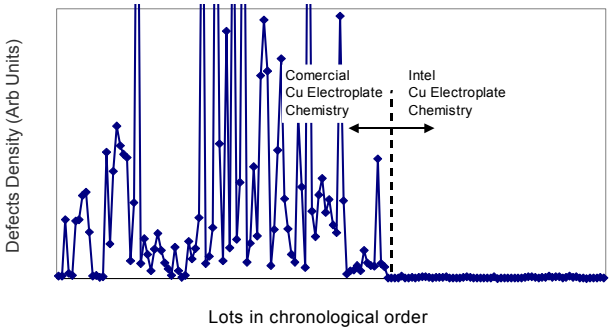


Figure 6. Impact of Intel Cu Plating Chemistry on Defect Density

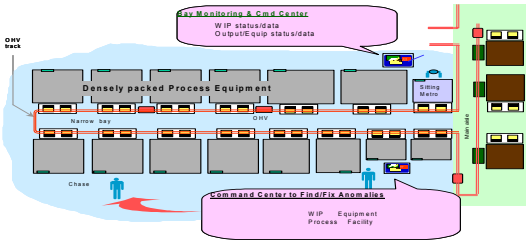


Figure 7. "Lights Out" 300mm Automation Infrastructure.

B. Design for Performance

To deliver high performance products, processes must deliver industry leading transistor delay. Intel consistently delivers the highest performance transistors in the industry (2). This is achieved by not only setting and delivering to aggressive technology targets but also by point use of advanced process control (APC) techniques in those areas where minimizing process variation delivers increased performance and reliability.

C. Design for Safety and Cost

Intel's first 300mm fab features the world's first fully automated system for handling wafers (4). Due to ergonomic concerns with 300mm wafers as well as the opportunity to reduce manufacturing cost, Intel's 300mm factories feature integrated point-to-point delivery capability and Overhead Hoist Vehicles (OHV's) that enable "lights out" operations (Fig. 7).

Industry Leading 200mm and 300mm Die Yields

Delivering low cost technologies means delivering processes at high die yields. Note that in Fig. 2 the 130nm generation defect learning rate for both 200mm and 300mm is the fastest to date with the technology already delivering die yields at mature technology levels. This is achieved through reliable projection of yield by in-line monitors and models, which enables yield learning without the need for fully integrated wafers.

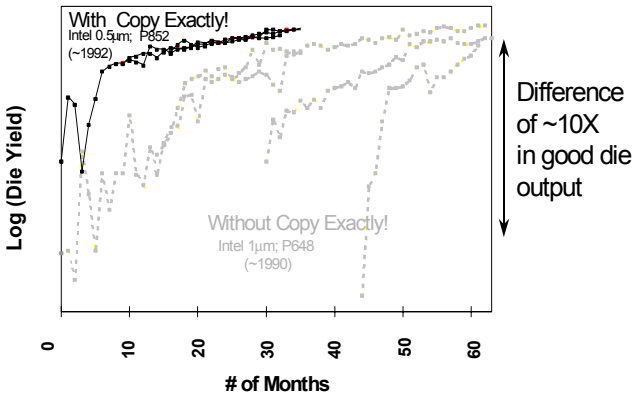
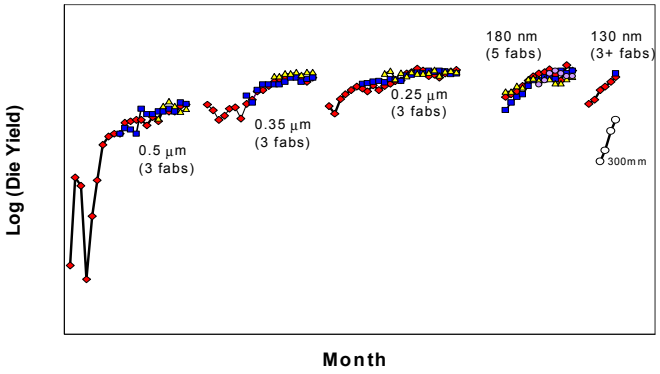


Figure 8. The Birth of Copy Exactly in the Late 1980's



Matched Die Yields During High Volume Ramp

Quick wafer ramps at high yields and transitioning processes to 300mm enhances competitiveness. Based on difficulties with fab transfers in the 80's (Fig. 8), Intel now uses Copy Exactly! methods for all fab technology transfer and ramp. Fig. 9 shows the results for Intel fab transfer and ramps from the 0.5µm down to the 130nm technology, including 300mm.

Matched 200mm and 300mm Production

A modified Copy Exactly! method was used for 130nm technology 300mm process transfer. In addition to "key process monitor" or output matching, partial recipe or input matching was used in cases where those input parameters were expected to impact yield, performance or reliability. The form, fit and function of the 200 and 300mm technologies are matched. Fig. 10 shows ring oscillator performance matching. Figs. 11 and 12 show gate oxide TTF and electromigration TTF matching results. Variability with 300mm is equivalent or better to 3mm edge exclusion as shown by the within wafer maps of via resistance and gate oxide thickness (Figs. 13 and 14). Fig. 15 shows transistor Idsat matching.

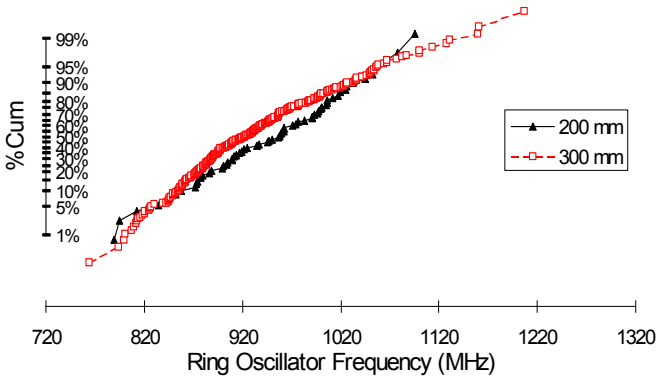


Figure 10. Ring Oscillator Performance 200mm/300mm Matching

Conclusion

Intel's 130nm logic technology has been ramped to high volume production in multiple factories and on both 200mm and 300mm production lines at record yields, quality and ramp rate. This technology has the best CMOS transistor performance currently in production and uses full Cu interconnect. Process design for manufacturing, continuous acceleration of the rate of development and use of Copy Exactly! transfer methods are the key elements that allow Intel continue to deliver highly competitive process technologies.

Acknowledgements

The author would like to thank the engineers and technicians in Portland Technology Development group that are responsible for development and transfer to manufacturing of Intel's logic technologies.

References

(1) G. Moore, "Intel Developers Keynote Address", 9/65.
(2) Tyagi, et al., IEDM Tech. Dig., pp. 567-570, (2000)
(3) Brewer, et al, VLSI Multi Int Dig, pp 376-84, 1987
(4) K. Srinivasan, Intel Technology Journal Q3, 2001.

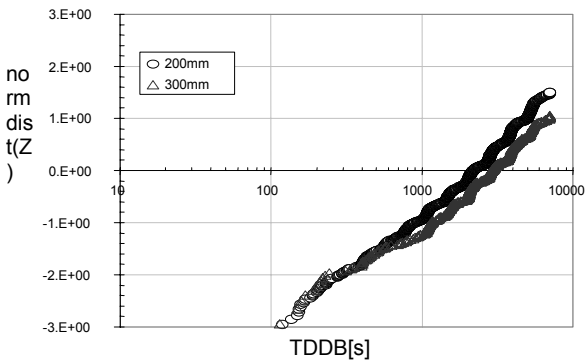


Figure 11 Gate Oxide TTF 200mm/300mm Matching

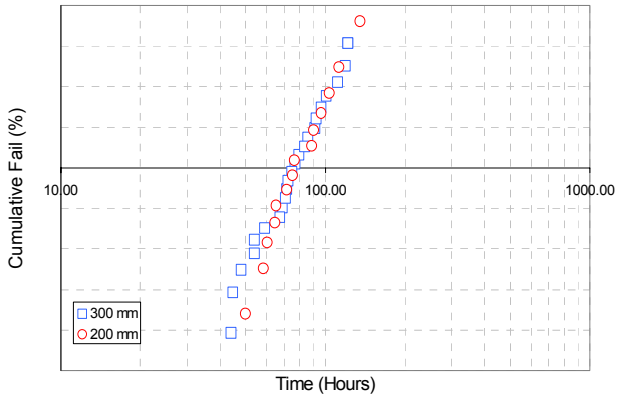


Figure 12 Electromigration TTF 200mm/300mm Matching

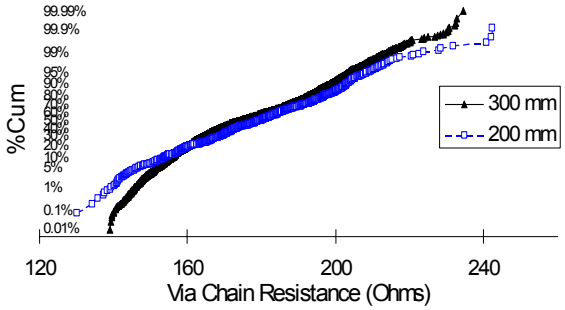


Figure 13 Via resistance Within Wafer 200mm/300mm Matching

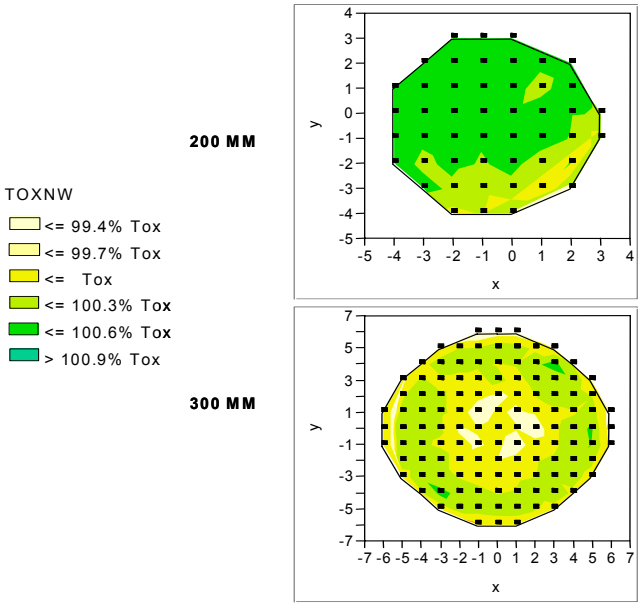


Figure 14. Gate Oxide Thickness Within Wafer 200mm/300mm Matching

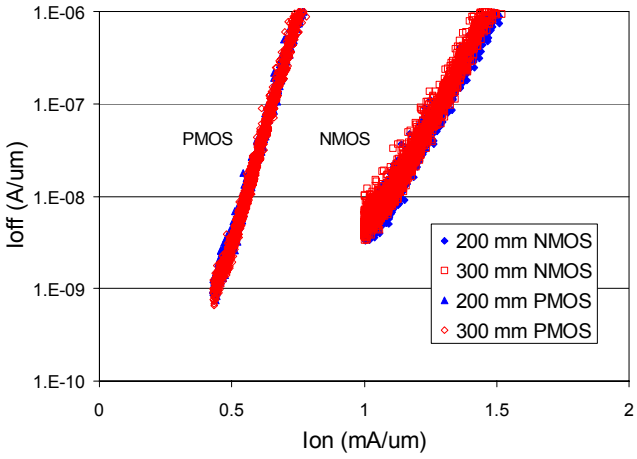


Figure 15. P and N-channel Idsat 200mm/300mm Matching